REMARKS

In response to the final Office Action dated May 10, 2010, the Assignee respectfully requests continued examination and reconsideration based on the above amendments and on the following remarks.

Claims 1, 5-14, 36, and 39-46 are pending in this application.

Rejection of Claims under § 103 (a)

The Office rejected claims 1, 5-6, 36, 39-41, and 44-46 under 35 U.S.C. § 103 (a) as being unpatentable over U.S. Patent 6,005,861 to Humpleman in view of U.S. Patent 6,493,875 to Eames, *et al.*, in view of U.S. Patent 6,732,366 to Russo, and further in view of U.S. Patent 4,809,069 to Meyer, *et al.*

These claims, though, are not obvious over *Humpleman*, *Eames*, *Russo*, and *Meyer*. These claims have been amended recite, or to incorporate, many features that are not disclosed or suggested by *Humpleman*, *Eames*, *Russo*, and *Meyer*. Independent claim 1, for example, recites "*a video overlay processor having an input connected to the media bus, another input connected to the system data bus, and an output connected to the system data bus*" (emphasis added). Support for these features may be found at least in the as-filed application at FIG. 6. Independent claim 36 recites similar features.

At least these features are not obvious over *Humpleman*, *Eames*, *Russo*, and *Meyer*. As the Assignee previously explained, *Humpleman* describes network interface units. *See* U.S. Patent 6,005,861 to Humpleman at column 3, lines 20-35. Digital signals from each network interface unit are distributed over an Ethernet network. *See id.* at column 3, lines 49-52. Each network interface unit connects to a scalable switch hub and thus to terminal units. *See id.* at column 3, lines 52-55. *Eames* describes a wireless gateway for use in a residence. *See* U.S. Patent 6,493,875 to Eames, *et al.* at column 1, lines 39-45. The gateway has a "network

interface module" that interfaces with a motherboard that contains a processor, memory, MPEG processor, and an Ethernet block. *See id.* at column 5, lines 1-7. "A set of buses" routes information "within [the] gateway." *See id.* at column 5, lines 25-29. *Russo* describes a storage device that stores video. When a program is retrieved and viewed, a subscriber is billed. *See* U.S. Patent 6,732,366 to Russo at column 3, lines 17-20 and at column 5, lines 12-25. Payment is only due when a majority of the program is watched. *See id.* at column 5, lines 35-40.

Meyer discloses a picture-in-picture processor. *Meyer's* "PIP" processor is connected to multiplexers, as *Meyer* illustrates in FIGS. 1a, 1b, and 2-11.

Still, though, the independent claims are not obvious over *Humpleman*, *Eames*, and *Russo*. The proposed combination of *Humpleman*, *Eames*, and *Russo* still fails to teach or suggest all the features of the independent claims, such as the "*video overlay processor having an input connected to the media bus, another input connected to the system data bus, and an output connected to the system data bus*" (emphasis added). While the proposed combination of *Humpleman*, *Eames*, *Russo*, and *Meyer* teaches a picture-in-picture processor, *Meyer's* picture-in-picture processor connects to multiplexers. *Humpleman*, *Eames*, *Russo*, and *Meyer's* picture-in-picture processor does not have "*an input connected to the media bus, another input connected to the system data bus, and an output connected to the system data bus*" (emphasis added). One of ordinary skill in the art, then, would not think that the independent claims are obvious.

Independent claim 36 recites even more distinguishing features. Independent claim 36, for example, recites "*each pair having an output connected to the system data bus and connected to an analog-to-digital converter, the multiple tuner and demodulator pairs sending an analog information signal to the analog-to-digital converter, and the analog-to-digital converter outputting digital information signal based at least in part on the analog information signal*." Support for these features may be found at least in the as-filed application at page 12, lines 12-15; at page 16, lines 19-22; and illustrated in FIG. 6. Independent claim 36 also recites "*the multiple tuner and demodulator pairs also connected to a decryption circuit that decrypts an*

encrypted information signal received from the multiple tuner and demodulator pairs and that produces a decrypted information signal." Support for these features may be found at least in the as-filed application at page 16, line 24; at page 21, lines 13-16; and illustrated in FIG. 6. Independent claim 36 also recites "*a decoder circuit connected to the decryption circuit that converts the decrypted information signal from one format to a second format*." Support for these features may be found at least in the as-filed application at page 17, lines 1-4; at page 21, lines 17-20; and illustrated in FIG. 6. Independent claim 36 also recites "*a cipher/decipher circuit connected to the decoder circuit and connected to the analog-to-digital converter that deciphers the digital information from the analog-to-digital converter and deciphers the converted decrypted information signal from the decoder circuit*." Support for these features may be found at least in the as-filed application at page 17, lines 9-15 and illustrated in FIG. 6. Independent claim 36 also recites "*the cipher/decipher circuit connected to a media bus and sending deciphered information signals to the media bus*." Support for these features may be found at least in the as-filed application at page 17, lines 9-15 and illustrated in FIG. 6. Independent claim 36 also recites "*the system data bus connected to the media bus and configured to only receive the deciphered information signals from the media bus, the system data bus unable to send information to the media bus*." Support for these features may be found at least in the as-filed application at FIG. 6. Because *Humpleman*, *Eames*, *Russo*, and *Meyer* remains silent to all these features, independent claim 36 cannot be obvious.

Claims 1, 5-6, 36, 39-41, and 44-46, then, are not obvious over *Humpleman*, *Eames*, *Russo*, and *Meyer*. The independent claims recite many distinguishing features, and the dependent claims incorporate these distinguishing features. One of ordinary skill in the art, then, would not think that claims 1, 5-6, 36, 39-41, and 44-46 are obvious. The Office is respectfully requested to remove the § 103 (a) rejection of these claims.

Traversal of "Official Notice"

The Assignee traverses Examiner Saltarelli's "Official Notice." Examiner Saltarelli takes "Official Notice" that because analog-to-digital converters are well known, *Humpleman* could

have been easily modified. *See* Examiner Saltarelli, Final Office Action mailed May 10, 2010, ay page 7, lines 13-21.

Whether or not this "Official Notice" is true, this is not what is claimed. Independent claim 36 recites "*connecting the multiple tuners to a system data bus and to an analog-to-digital converter*," "*sending the analog information signal to the analog-to-digital converter*," and "*outputting a digital information signal from the analog-to-digital converter that is based at least in part on the analog information signal*." Even if analog-to-digital converters are well known, Examiner Saltarelli makes no assertion that the claimed circuit architecture is well known. Indeed, Examiner Saltarelli's "Official Notice" wholly lacks any consideration of the claimed circuit architecture. The Assignee thus respectfully disagrees with Examiner Saltarelli's assertion of "Official Notice." Examiner Saltarelli is respectfully requested to re-examine independent claim 36 in light of the claimed circuit architecture.

If Examiner Saltarelli maintains an assertion of Official Notice, the Assignee respectfully demands production of documentary evidence to support the assertion, as M.P.E.P. § 2144.04 (C) provides.

Rejection of Claims 7 & 42 under § 103 (a)

The Office rejected claims 7 and 42 under 35 U.S.C. § 103 (a) as being obvious over *Humpleman*, *Eames*, *Russo*, and *Meyer* and further in view of U.S. Patent 5,768,527 to Zhu, *et al.* Claims 7 and 42, however, depend, respectively, from independent claims 1 and 36. *Humpleman*, *Eames*, *Russo*, and *Meyer* fails to teach or suggest all the features of independent claims 1 and 36, and *Zhu* does not cure the deficiencies. *Zhu* discloses a "rate scaler" that reduces bit rates of input streams. Still, though, *Humpleman* with *Eames*, *Russo*, *Meyer*, and *Zhu* still fails to fails to teach or suggest all the features of independent claims 1 and 36. One of ordinary skill in the art, then, would not think that claims 7 and 42 are obvious. The Office is respectfully requested to remove the § 103 (a) rejection of these claims.

Rejection of Claims 8-14 & 43 under § 103 (a)

Claims 8-14 and 43 were also rejected under 35 U.S.C. § 103 (a) as being obvious over *Humpleman*, *Eames*, *Russo*, and *Meyer* and further in view of U.S. Patent 6,104,861 to Tsukagoshi and further in view of U.S. Patent 5,473,772 to Halliwell, *et al.*

Claims 8-14 and 43, though, depend from either independent claim 1 or 36. The paragraphs above explained that *Humpleman*, *Eames*, and *Russo* fails to teach or suggest all the features of independent claims 1 and 36, and neither *Tsukagoshi* nor *Halliwell* cure their deficiencies. The rejection of these claims must fail, so the Office is respectfully requested to remove the § 103 (a) rejection of these claims.

If any questions arise, the Examiner is invited contact the undersigned at (919) 469-2629 or scott@scottzimmerman.com.

Respectfully submitted,

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